

CLAIMS

What is claimed is:

- 1 1. A preamplifier system, comprising:
 - 2 (a) a magneto-resistive (MR) sensor;
 - 3 (b) an alternating current (AC) coupling module coupled to the MR sensor for
4 blocking a direct current (DC) voltage associated with an input signal, and
5 filtering low frequency noise associated with the input signal;
 - 6 (c) a gain stage module coupled to the AC coupling module, the gain stage module
7 including a plurality of cascode field effect transistors (FETs) configured for
8 amplifying the input signal, while reducing intrinsic noise and increasing
9 operational bandwidth; and
 - 10 (d) a control circuit coupled to the gain stage module for feeding back an output of
11 the gain stage module.
- 1 2. The system as recited in claim 1, wherein one of the cascode FETs includes a
2 dimension ratio (width/length) with a value of at least 4000.

1 3. The system as recited in claim 1, wherein the gain stage module includes a first
2 transistor including a source terminal coupled to ground, a gate terminal, and a
3 drain terminal; a second transistor including a source terminal coupled to the drain
4 terminal of the first transistor, a gate terminal, and a drain terminal coupled to the
5 output of the gain stage module; a third transistor including a source terminal
6 coupled to the drain terminal of the second transistor, a gate terminal coupled to
7 the power source, and a drain terminal coupled to the power source; a fourth
8 transistor including a source terminal coupled to ground, a gate terminal coupled
9 to the drain terminal of the first transistor, and a drain terminal coupled to the gate
10 terminal of the second transistor; a fifth transistor including a source terminal
11 coupled to the power source, a gate terminal, and a drain terminal coupled to the
12 drain terminal of the fourth transistor and the gate terminal of the second
13 transistor; and a capacitor coupled between ground and the drain terminal of the
14 fifth transistor, the drain terminal of the fourth transistor, and the gate terminal of
15 the second transistor.

1 4. The system as recited in claim 3, wherein the AC coupling module includes a
2 capacitor including a first terminal coupled to the gate terminal of the first
3 transistor and the MR sensor.

1 5. The system as recited in claim 3, wherein the control circuit includes an
2 operational transductance amplifier with a first input coupled to the output of the
3 gain stage module and a second input coupled to a reference output, the

4 operational transductance amplifier including an output coupled to a gate terminal
5 of a sixth transistor including a source terminal coupled to the power source, and
6 a drain terminal, the control circuit further including a first resistor having a first
7 terminal coupled to the drain terminal of the sixth transistor and a second terminal
8 coupled to the gate terminal of the first transistor, a second resistor including a
9 first terminal coupled to the drain terminal of the sixth transistor and a second
10 terminal coupled to ground.

1 6. The system as recited in claim 5, wherein the reference output is defined by an
2 eighth transistor including a source terminal, a gate terminal, and a drain terminal
3 coupled to the reference output; a ninth transistor including a source terminal
4 coupled to the reference output, a gate terminal coupled to the power source, and
5 a drain terminal coupled to the power source; and a current source including a
6 first terminal coupled to the source terminal of the eighth transistor and a second
7 terminal coupled to ground.

1 7. The system as recited in claim 3, wherein a gain at the drain terminal of the first
2 transistor is less than one (1).
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1 8. A preamplifying method, comprising:

- 2 (a) receiving an input signal from a magneto-resistive (MR) sensor;
3 (b) blocking a direct current (DC) voltage associated with the input signal;

- 4 (c) filtering low frequency noise associated with the input signal;
- 5 (d) amplifying the input signal utilizing a plurality of cascode field effect transistors
- 6 (FETs); and
- 7 (e) feeding back an output of the amplification utilizing a control circuit.

1 9. A preamplifier circuit, comprising:

2 a first transistor including a source terminal coupled to ground, a gate terminal,

3 and a drain terminal;

4 a second transistor including a source terminal coupled to the drain terminal of the

5 first transistor, a gate terminal, and a drain terminal coupled to an output;

6 a third transistor including a source terminal coupled to the drain terminal of the

7 second transistor, a gate terminal coupled to the power source, and a drain terminal

8 coupled to the power source;

9 a fourth transistor including a source terminal coupled to ground, a gate terminal

10 coupled to the drain terminal of the first transistor, and a drain terminal coupled to the

11 gate terminal of the second transistor;

12 a fifth transistor including a source terminal coupled to the power source, a gate

13 terminal, and a drain terminal coupled to the gate terminal of the second transistor and the

14 drain terminal of the fourth transistor; and

15 a capacitor coupled between ground and the drain terminal of the fifth transistor,

16 the drain terminal of the fourth transistor, and the gate terminal of the second transistor.

- 1 10. The preamplifier circuit as recited in claim 9, wherein the first transistor includes
2 a field effect transistor (FET).
- 1 11. The preamplifier circuit as recited in claim 10, wherein the first transistor includes
2 a dimension ratio (width/length) with a value of at least 4000.
- 1 12. The preamplifier circuit as recited in claim 9, and further comprising a sixth
2 transistor including a source terminal coupled to the power source, a gate
3 terminal, and a drain terminal.
- 1 13. The preamplifier circuit as recited in claim 12, and further comprising a seventh
2 transistor including a source terminal coupled to the power source, a gate
3 terminal, and a drain terminal coupled to a magneto-resistive (MR) sensor.
- 1 14. The preamplifier circuit as recited in claim 13, and further comprising an eighth
2 transistor including a source terminal, a gate terminal, and a drain terminal
3 coupled to a second output.
- 1 15. The preamplifier circuit as recited in claim 14, and further comprising a ninth
2 transistor including a source terminal coupled to the second output, a gate
3 terminal coupled to the power source, and a drain terminal coupled to the power
4 source.

1 16. The preamplifier circuit as recited in claim 15, and further comprising an
2 operational transductance amplifier with a first input coupled to the first output
3 and a second input coupled to the second output, the operational transductance
4 amplifier including an output coupled to the gate terminal of the sixth transistor.

1 17. The preamplifier circuit as recited in claim 16, and further comprising a first
2 current source including a first terminal coupled to the source terminal of the
3 eighth transistor and a second terminal coupled to ground.

1 18. The preamplifier circuit as recited in claim 17, and further comprising a second
2 current source including a first terminal coupled to the power source and a second
3 terminal coupled to the gate terminal of the fourth transistor.

1 19. The preamplifier circuit as recited in claim 18, and further comprising another
2 capacitor including a first terminal coupled to the gate terminal of the first
3 transistor and a second terminal coupled to a magneto-resistive (MR) sensor.

1 20. A preamplifier circuit system, comprising:
2 a magneto-resistive (MR) sensor including a first terminal coupled to ground and
3 a second terminal;
4 a first transistor including a source terminal coupled to ground, a gate terminal
5 coupled to a first node, and a drain terminal;

6 a second transistor including a source terminal coupled to the drain terminal of the
7 first transistor, a gate terminal coupled to a second node, and a drain terminal coupled to
8 a first output;

9 a third transistor including a source terminal coupled to the drain terminal of the
10 second transistor, a gate terminal coupled to a power source, and a drain terminal coupled
11 to the power source;

12 a fourth transistor including a source terminal coupled to ground, a gate terminal
13 coupled to the drain terminal of the first transistor, and a drain terminal coupled to the
14 second node;

15 a fifth transistor including a source terminal coupled to the power source, a gate
16 terminal, and a drain terminal coupled to the second node;

17 a sixth transistor including a source terminal coupled to the power source, a gate
18 terminal, and a drain terminal coupled to a third node;

19 a seventh transistor including a source terminal coupled to the power source, a
20 gate terminal, and a drain terminal coupled to the second terminal of the MR sensor;

21 an eighth transistor including a source terminal, a gate terminal, and a drain
22 terminal coupled to a second output;

23 a ninth transistor including a source terminal coupled to the second output, a gate
24 terminal coupled to the power source, and a drain terminal coupled to the power source;

25 an operational transductance amplifier with a first input coupled to the first output
26 and a second input coupled to the second output, the operational transductance amplifier
27 including an output coupled to the gate terminal of the sixth transistor;

28 a first current source including a first terminal coupled to the source terminal of
29 the eighth transistor and a second terminal coupled to ground;
30 a second current source including a first terminal coupled to the power source and
31 a second terminal coupled to the gate terminal of the fourth transistor;
32 a first capacitor including a first terminal coupled to the power source and a
33 second terminal coupled to the gate terminal of the sixth transistor;
34 a second capacitor including a first terminal coupled to the second node and a
35 second terminal coupled to ground;
36 a third capacitor including a first terminal coupled to the first node and a second
37 terminal coupled to the second terminal of the MR sensor;
38 a first resistor including a first terminal coupled to the third node and a second
39 terminal coupled to the first node; and
40 a second resistor including a first terminal coupled to the third node and a second
41 terminal coupled to ground.

1 21. A disk drive system, comprising:
2 a magnetic recording disk;
3 a magnetic head including an magneto-resistive (MR) sensor;
4 an actuator for moving the magnetic head across the magnetic recording disk so
5 the magnetic head may access different regions of the magnetic recording disk; and
6 a controller electrically coupled to the magnetic head including a preamplifier
7 including:

8 an alternating current (AC) coupling module coupled to the MR sensor for
9 blocking a direct current (DC) voltage associated with an input signal, and
10 filtering low frequency noise associated with the input signal,
11 a gain stage module coupled to the AC coupling module, the gain stage
12 module including a plurality of cascode field effect transistors (FETs) configured
13 for amplifying the input signal, while reducing intrinsic noise and increasing
14 operational bandwidth, and
15 a control circuit coupled to the gain stage module for feeding back an
16 output of the gain stage module.